EXHIBIT A

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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
61/047,274	04/23/2008		105	13054-285		

CONFIRMATION NO. 1135

FILING RECEIPT

32841
BAHRET & ASSOCIATES
320 NORTH MERIDIAN STREET
SUITE 510
INDIANAPOLIS, IN 46204

OC00000029636860

Date Mailed: 04/29/2008

Receipt is acknowledged of this provisional patent application. It will not be examined for patentability and will become abandoned not later than twelve months after its filing date. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please write to the Office of Initial Patent Examination's Filing Receipt Corrections. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Applicant(s)

James A. Cooper, West Lafayette, IN;
Asmita Saha, Hillsboro, OR;

Power of Attorney:
William Bahret--31087

If Required, Foreign Filing License Granted: 04/29/2008
The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 61/047,274**
Projected Publication Date: None, application is not eligible for pre-grant publication
Non-Publication Request: No
Early Publication Request: No
**** SMALL ENTITY ****
Title

SiC Power DMOSFETs with Self-Aligned Source Contacts

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

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Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

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Doc Code: **TR.PROV**
Document Description: Provisional Cover Sheet (SB16)

PTO/SB/16 (04-07)
Approved for use through 06/30/2010 OMB 0651-0032
U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

Provisional Application for Patent Cover Sheet

This is a request for filing a PROVISIONAL APPLICATION FOR PATENT under 37 CFR 1.53(c)

Inventor(s)

Inventor 1 — Remove

Given Name	Middle Name	Family Name	City	State	Country
James	A.	Cooper	West Lafayette	IN	US

Inventor 2 — Remove

Given Name	Middle Name	Family Name	City	State	Country
Asmita		Saha	Hillsboro	OR	US

All Inventors Must Be Listed – Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. — Add

Title of Invention	SiC Power DMOSFETs with Self-Aligned Source Contacts
Attorney Docket Number (if applicable)	13054-285

Correspondence Address

Direct all correspondence to (select one):

◉ The address corresponding to Customer Number	○ Firm or Individual Name
Customer Number	32841

The invention was made by an agency of the United States Government or under a contract with an agency of the United States Government.

○ No.

◉ Yes, the name of the U.S. Government agency and the Government contract number are:

DARPA #N000140510437; US Army TACOM #W56HZV06C0028

Doc Code: **TR.PROV**
Document Description: Provisional Cover Sheet (SB16)

PTO/SB/16 (04-07)
Approved for use through 06/30/2010 OMB 0651-0032
U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE
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Entity Status

Applicant claims small entity status under 37 CFR 1.27

- (•) Yes, applicant qualifies for small entity status under 37 CFR 1.27
- ( ) No

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Signature

Please see 37 CFR 1.4(d) for the form of the signature.

Signature	/William F. Bahet/			Date (YYYY-MM-DD)	Apr 23, 2008
First Name	William	Last Name	Bahret	Registration Number (If appropriate)	31087

This collection of information is required by 37 CFR 1.51. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 8 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **This form can only be used when in conjunction with EFS-Web. If this form is mailed to the USPTO, it may cause delays in handling the provisional application.**

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7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
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SiC POWER DMOSFETs WITH SELF-ALIGNED SOURCE CONTACTS

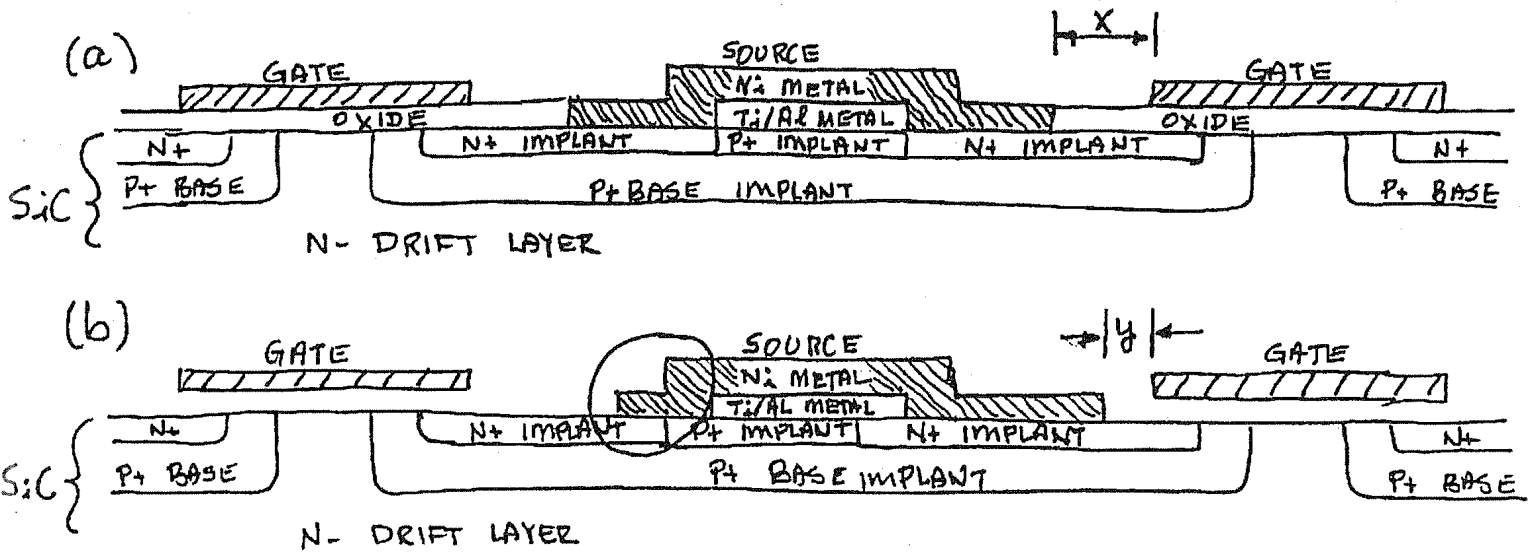
This application relates to SiC power DMOSFETs and is directed toward reducing the area of the transistor and the variations due to alignment tolerances such as mask misalignments. Among other applications, the invention is believed to be useful for electronic power switching, regulation and control, as well as motor drivers and power converters.

This application includes the attached paper and incorporates by reference all references cited therein.

SiC Power DMOSFETs with Self-Aligned Source Contacts

In power DMOSFETs, an important performance parameter is the specific on-resistance ($R_{ON,SP}$), which is defined as the product of the resistance in the linear region (low V_{DS}) times the area of the device (units are $\Omega\text{-cm}^2$ or $m\Omega\text{-cm}^2$). Thus it is important to minimize both the resistance and the area of the device. For DMOSFETs in the blocking voltage regime of 600 - 1800 V, a significant component of the total resistance is the resistance of the source contacts. Larger-area source contacts obviously have lower resistance, but increasing the contact area increases the total area of the device, and hence $R_{ON,SP}$. It is important to find ways to reduce the source contact resistance without increasing the area of the device. In a conventional DMOSFET, the source contact is defined by photolithography, and the source contact must be separated from the edge of the gate by sufficient distance so that the source contact and gate cannot touch even under worst-case misalignment of the source contact mask. In addition, the actual functional

area of the source contact is determined by the overlap of the source contact metal and the N+ implant that forms the source region in the semiconductor. Since the N+ implant is defined by a separate mask, the relative misalignment of the source contact mask and the N+ implant mask can reduce the functional area of the source contact, thereby increasing source resistance and degrading performance. The two cases of (a) perfectly aligned masks, and (b) worst-case misaligned masks are illustrated below. Here the Ni metal for the source contact

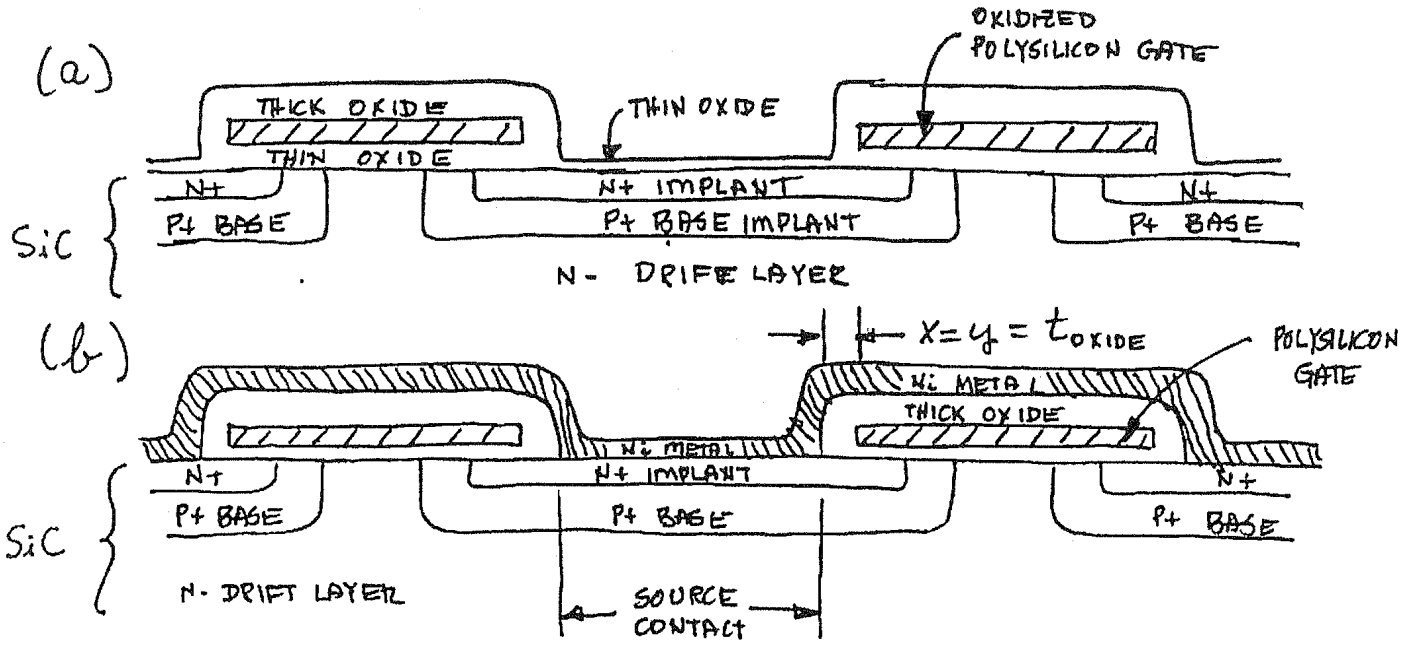


has been mis-aligned to the right (drawing b) and the P+ implant for the P+ base contact has been misaligned to the left. The resulting overlap of Ni metal and N+ implant in the circled area has been reduced almost to zero,

resulting in a very large contact resistance for this part of the device. Another drawback of this approach is the alignment tolerance (spacing x) that must be included in the design to insure that the source metal never comes into contact with the gate under worst-case misalignment (spacing y). The necessary inclusion of spacing x increases the area of the cell, increasing $R_{ON,SP}$. Both these problems can be eliminated by the <u>self-aligned source contact</u>, to be described next.

In this procedure, we employ a polycrystalline silicon (polysilicon) gate, and take advantage of the fact that polysilicon forms a much thicker SiO_2 layer than SiC when thermally oxidized at temperatures in the 850-1000 °C range. We then remove the SiO_2 over the SiC by a short oxide etch <u>without</u> using a photomask to define the area where the oxide is removed. Because it is much thicker, the oxide over the polysilicon gate is <u>not</u> completely

removed during this process, and the remaining oxide forms an insulating layer over the polysilicon gate. As part of this process, we assume the use of a segmented P+ contact to the P+ base, as described in an earlier patent disclosure by Cooper and Saha, and as already demonstrated experimentally (see, for example, A. Saha and J.A. Cooper, "A 1200 V 4H-SiC Power DMOSFET with Ultra-Low On-Resistance," IEEE Transactions on Electron Devices, 54, 2786-2791, Oct. 2007 or A. Saha and J.A. Cooper, "Optimum Design of Short-Channel 4H-SiC Power DMOSFETs," Materials Science Forum, 527-529, 1269-1272, 2006). Because the P+ contact only occurs in certain spots along the length of the source fingers, typically occupying around 10-15% of the finger length, the vast majority of the source fingers have no P+ contact, and the full area is available for use as N+ source contact. The drawings on the next page illustrate the structure and fabrication process. Drawing (a) shows the structure after the polysilicon gate has been oxidized but before the short oxide etch. Drawing (b) shows the structure after the short oxide etch has removed the oxide



over the SiC and often Ni ohmic contact metal has been deposited. Note that the Ni metal covers the <u>whole area</u>, overlapping the polysilicon gates but insulated from them by the thick oxide. The area of the functional source contact is <u>not</u> determined by the alignment of any masking levels and is <u>not</u> subject to random misalignments during processing. Instead, it is totally determined by the spacing between adjacent polysilicon gates, and is in fact <u>self-aligned</u> to the gate level, being separated by the thickness of the oxide layer covering the gate. This eliminates the alignment tolerance (X or y in the drawing on p. 5), reducing the cell area and the specific on-resistance.

This process has been tested experimentally and has already been incorporated into large-area power DMOSFETs.

Electronic Patent Application Fee Transmittal

Application Number:	
Filing Date:	
Title of Invention:	SiC POWER DMOSFETs WITH SELF-ALIGNED SOURCE CONTACTS
First Named Inventor/Applicant Name:	James A. Cooper
Filer:	William F. Bahret/Joyce Eden
Attorney Docket Number:	

Filed as Small Entity

Provisional Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Provisional Application filing fee	2005	1	105	105
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
		Total in USD ($)		**105**

Electronic Acknowledgement Receipt

EFS ID:	3197823
Application Number:	61047274
International Application Number:	
Confirmation Number:	1135
Title of Invention:	SiC POWER DMOSFETs WITH SELF-ALIGNED SOURCE CONTACTS
First Named Inventor/Applicant Name:	James A. Cooper
Customer Number:	32841
Filer:	William F. Bahret/Joyce Eden
Filer Authorized By:	William F. Bahret
Attorney Docket Number:	
Receipt Date:	23-APR-2008
Filing Date:	
Time Stamp:	16:32:31
Application Type:	Provisional

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$105
RAM confirmation Number	1731
Deposit Account	502176
Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes) /Message Digest	Multi Part /.zip	Pages (if appl.)

1	Provisional Cover Sheet (SB16)	ProvisionalSB.pdf	673754 42613e2883ebaee8c947aad746e6efce7716fe9f	no	3
Warnings:					
Information:					
2	Specification	ProvAppn.PDF	349151 7fca139a63a8530c981216df3e199d16f4bbfd25	no	7
Warnings:					
Information:					
3	Fee Worksheet (PTO-06)	fee-info.pdf	8125 eaffb7b6068ef1108e52fc3f9f7b923627e8e3bb	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	1031030		

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New International Application Filed with the USPTO as a Receiving Office
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